**Assignments on Basic gates**

1. AND gate

Symbol:

|  |  |  |  |
| --- | --- | --- | --- |
| http://electrosofts.com/verilog/and.jpg  Truth table: | | | |
|
| **A** | **B** | **Y** | |
| 0 | 0 | 0 | |
| 0 | 1 | 0 | |
| 1 | 0 | 0 | |
| 1 | 1 | 1 | |

y = a & b;

**OR GATE:**

module or\_gate(

    input a,

    input b,

    output c );

assign c=a | b;

endmodule

Symbol:

Truth table:

**NOT GATE:**

module not\_gate(

    input a,

    output c );

assign c=~a;

endmodule

Symbol:

Truth table:

**NOR GATE:**

module nor\_gate(

    input a,

    input b,

    output c );

assign c=~(a | b);

endmodule

Symbol:

Truth table:

**XOR GATE:**

module xor\_gate(

    input a,

    input b,

    output c );

assign c=a ^ b;

endmodule

Symbol:

Truth table:

**XNOR GATE:**

module xnor\_gate(

    input a,

    input b,

    output c );

assign c=~(a ^ b);

endmodule

Symbol:

Truth table:

**NAND GATE:**

module and\_gate(

    input a,

    input b,

    output c );

assign c=~(a&b);

endmodule

Symbol:

Truth table: